Design and implementation of RF power amplifier for Zigbee nodes

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Supervisor:

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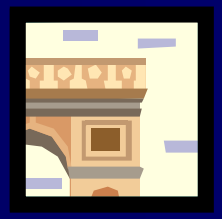
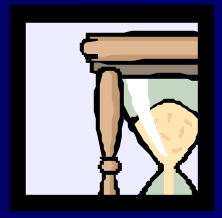
Outline



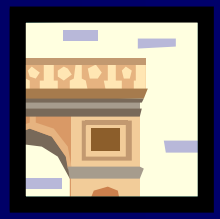
Introduction / objectives

Design



Simulations

Conclusions / future work and questions



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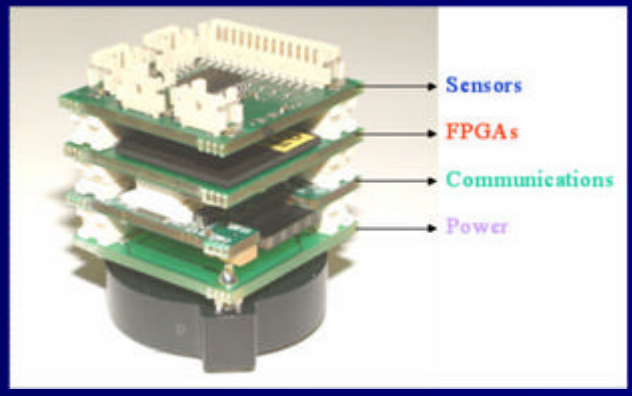
Introduction



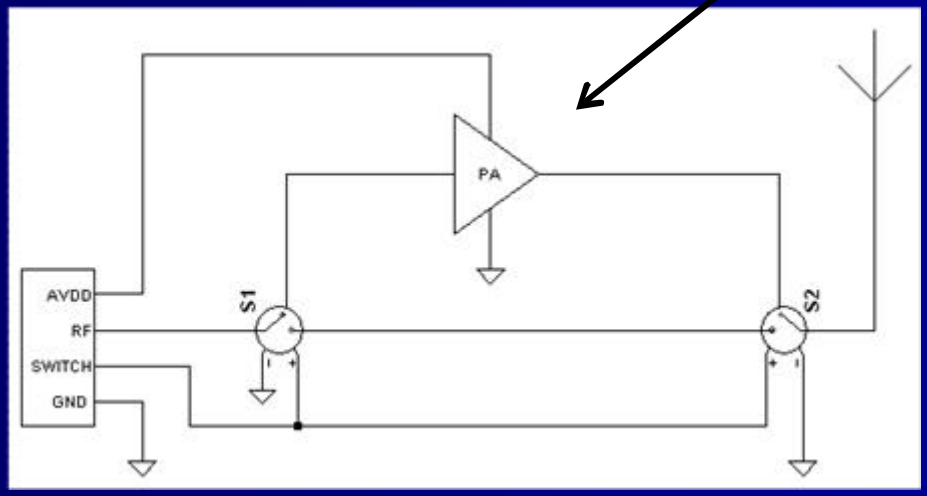
- Wireless modular Zigbee node
- Dimensions 25mm square
- 2400–2483.5MHz
- Transmit power 1mW max

Introduction

2nd Design:
Transistor level design

Class A max. PAE=50%
Class B max. PAE=78.5%

Power amplifier
Class AB or B



New RF layer

Objectives

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Supply Voltage		AV_{DD}	3.1	3.3	3.5	V
2	Output power	BW=2MHz	P_{out}		12		dBm
3	Spurious emission		P_{SP}			-80	dBm /Hz
4	PAE	@ max power		23%			mA
5	Gain			12			dB

Electrical parameters

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	PCB dimensions					25x25	mm

Mechanical parameters

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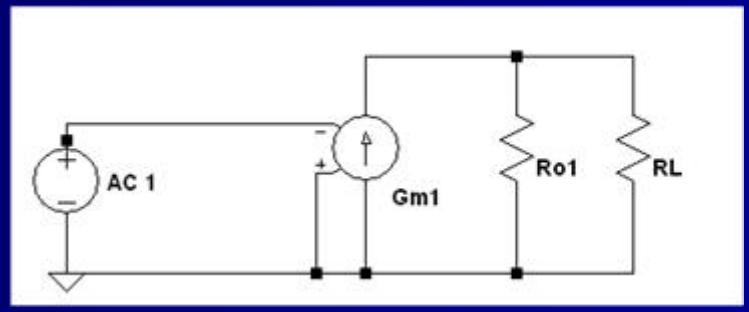
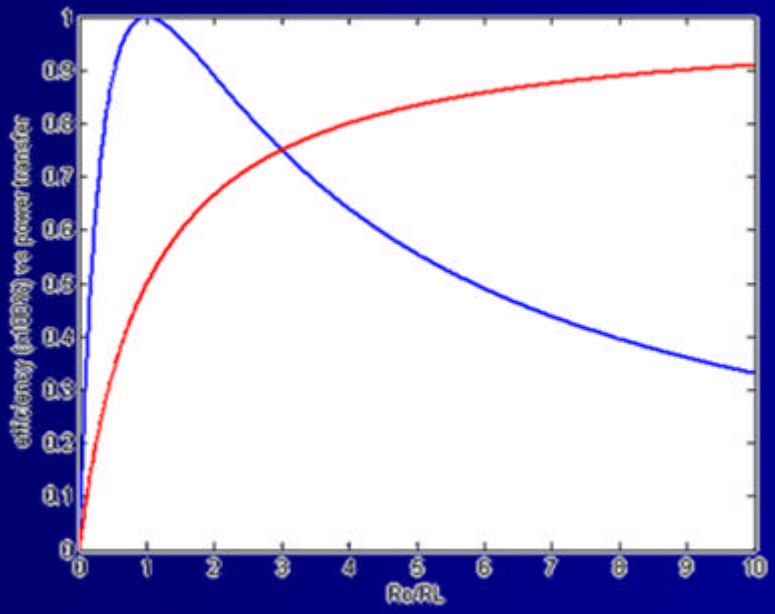
Design

- Architecture
- Input impedance matching
- Load impedance transformation
- Output filter
- Auto-bias




Architecture

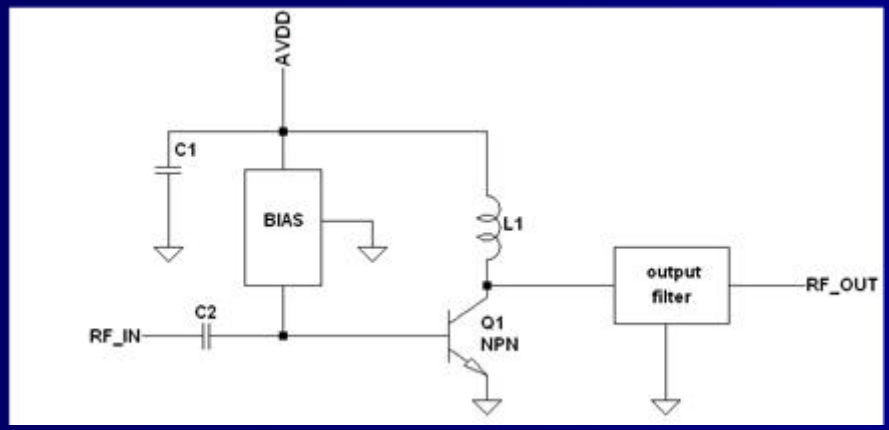




Ro/RI ⟶

Efficiency (red) versus power transfer (bleu)

Architecture



BFP640F BJT of Infineon has Been chosen based on S_{21}

$$P_{\max} = \frac{\left(\frac{V_{DD}}{\sqrt{2}}\right)^2}{R_{in}} = \frac{V_{DD}^{\ 2}}{2 \cdot R_{in}}$$

Rload=270? for max. efficiency

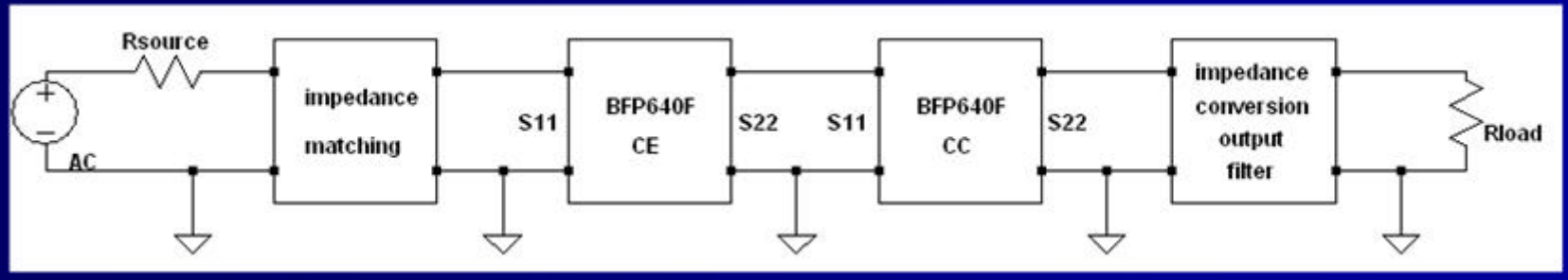
Three problems arise:

- Input impedance varies quite severe
- Rload > Rout
- Gain is not sufficient

Solution: Two stages

Architecture

	Common collector (CC)	Common emitter (CE)
pros	Relative high input impedance	Voltage gain > 1
	Relative low output impedance	Manufacturers s-parameters available
cons	Prone to oscillations	Prone to oscillations
	Voltage gain < 1	Relative low input impedance
	No manufacturers S parameters available	Cascode needed for good efficiency
	Vbe voltage drop	Reduced headroom



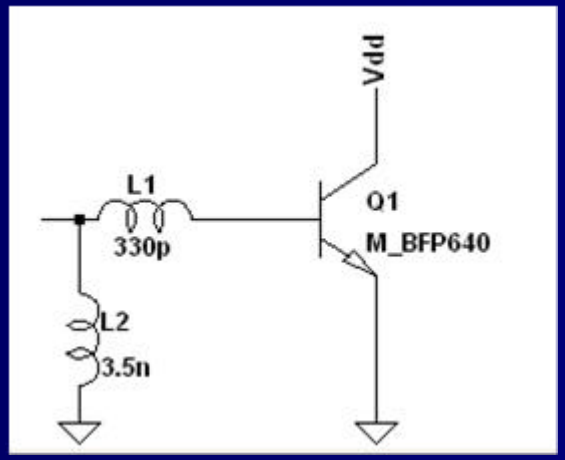
New Rload=200? for max. efficiency

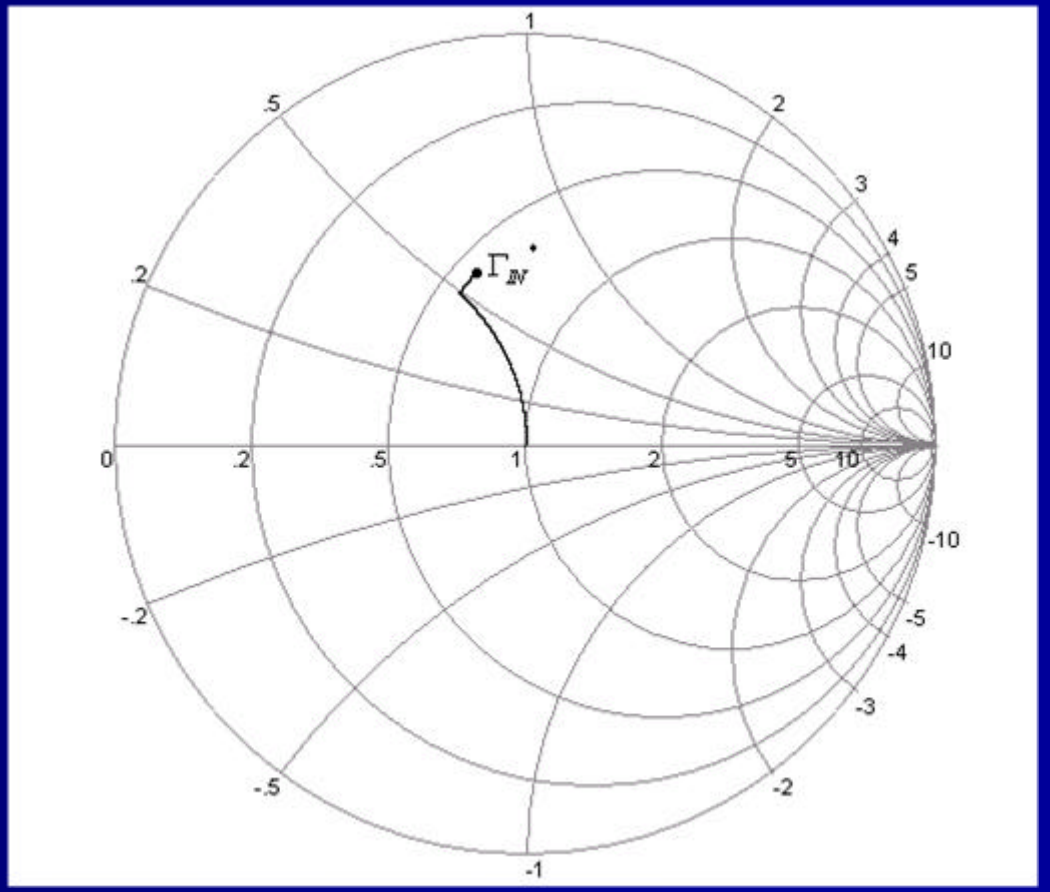
Input impedance matching

Unilateral figure of merit is too high for the BFP640F ——— Bilateral design

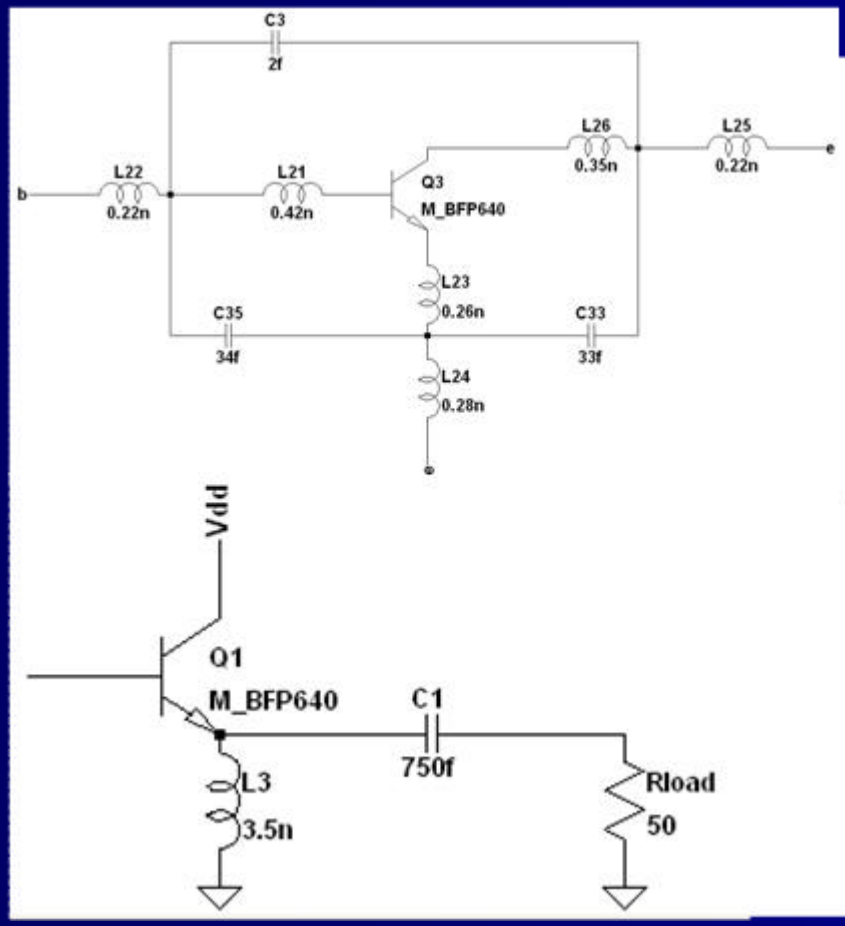
Bilateral input
Reflection coefficient:

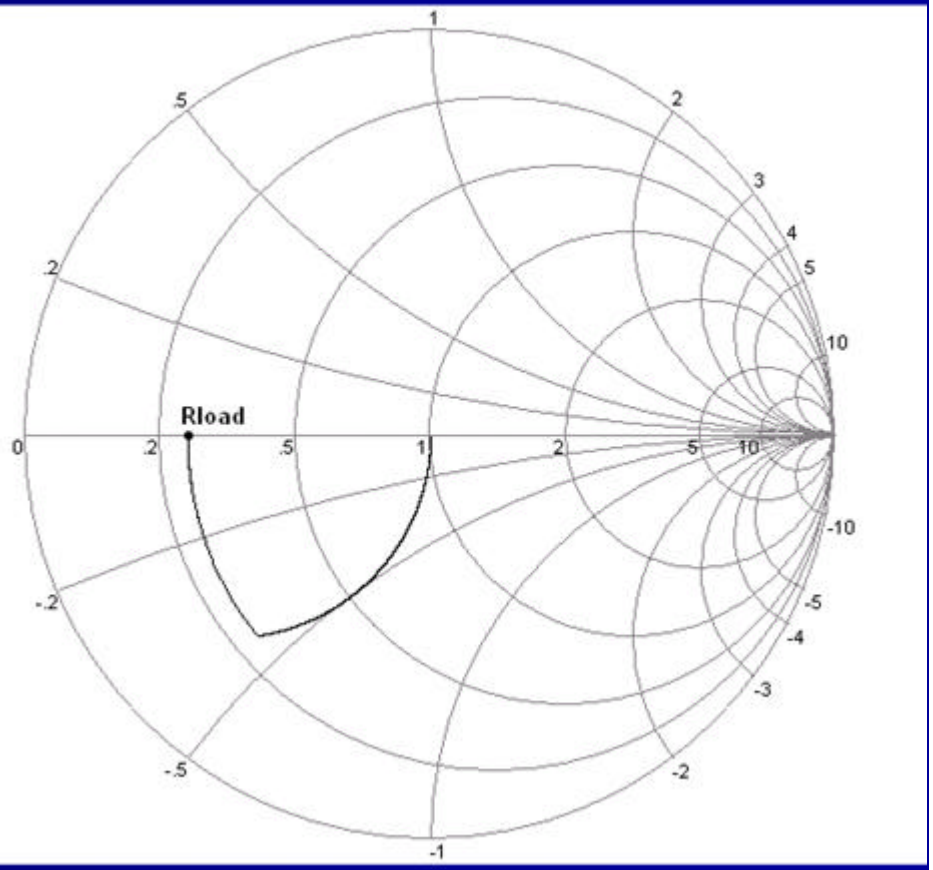
$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_{IN}}$$





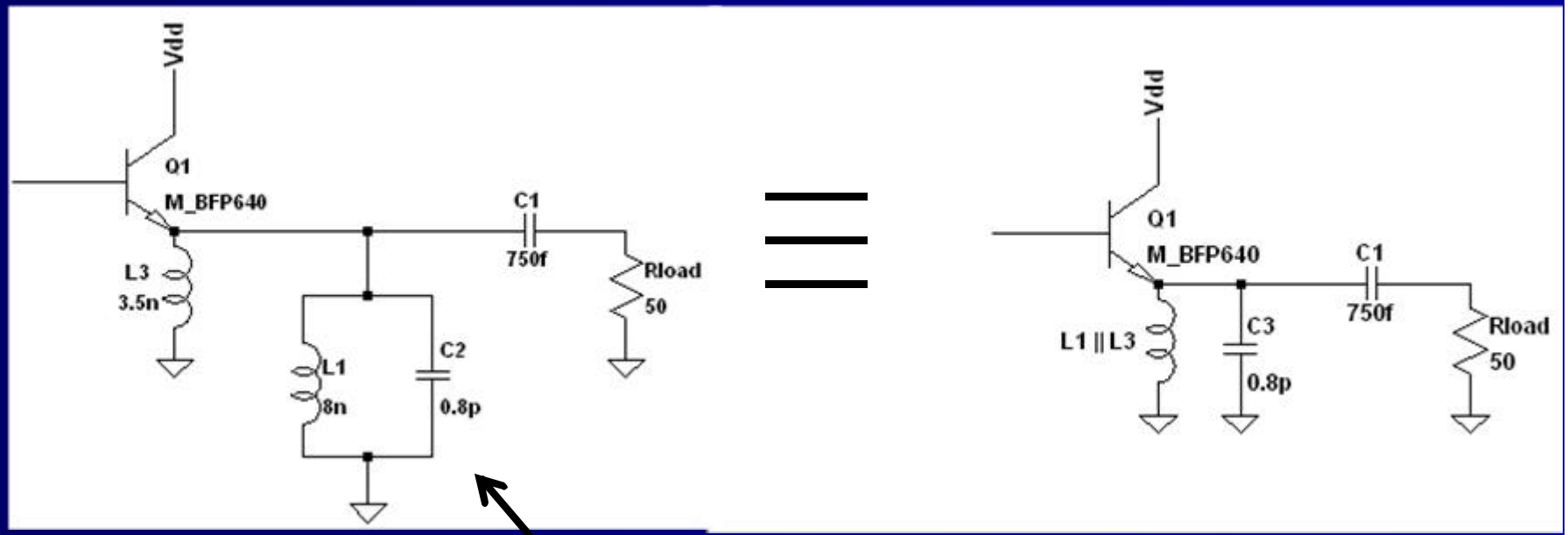
Load impedance transformation





Smith chart, normalised to 200?

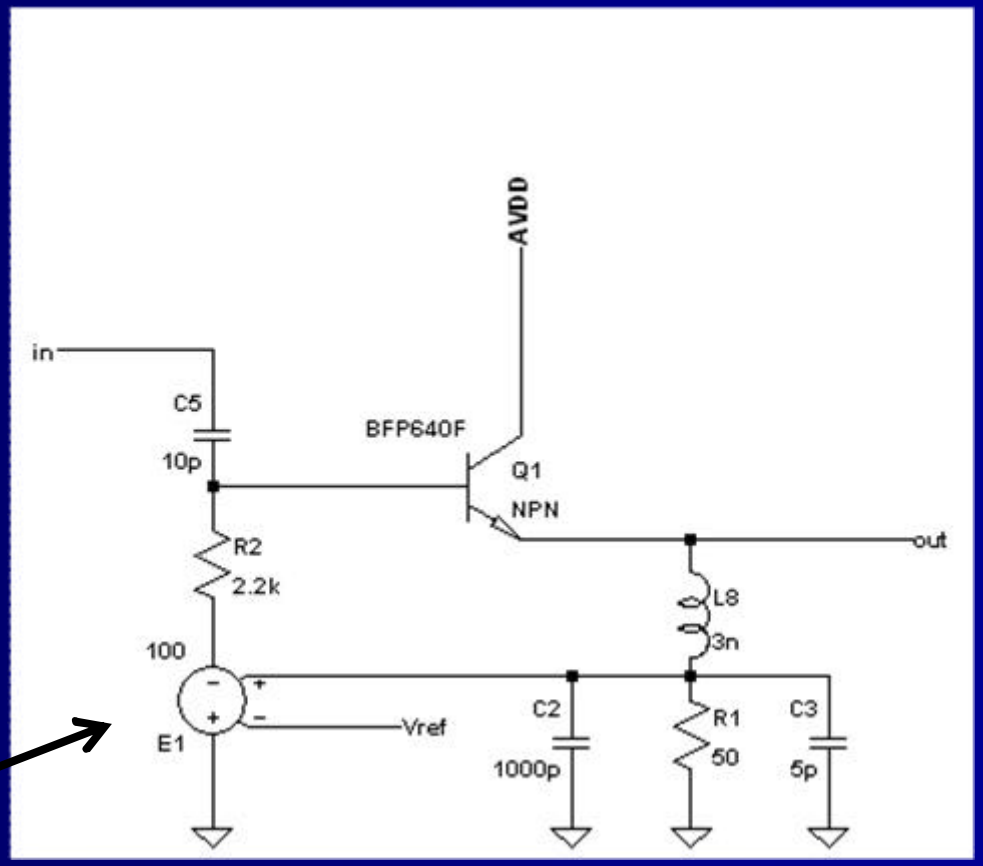
Output filter



Resonance network

Auto-bias

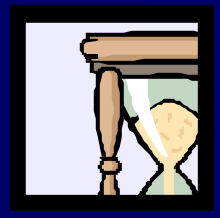


Op-amp

Introduction / objectives

Design



Simulations

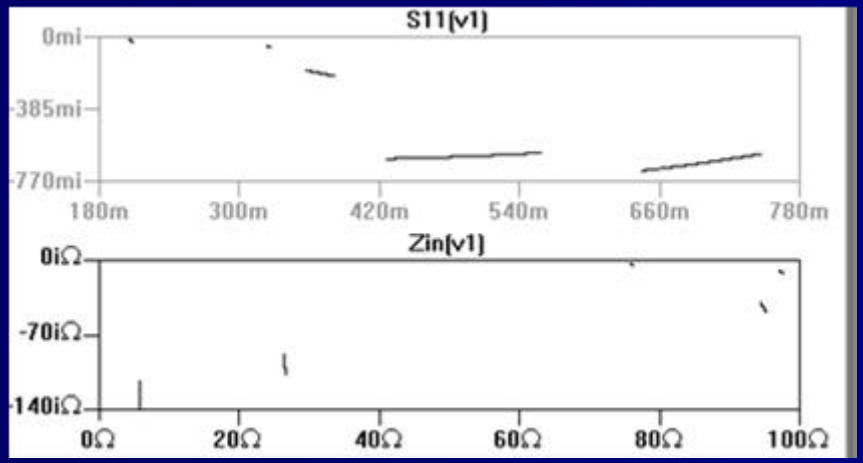
Conclusions / future work and questions

Simulations

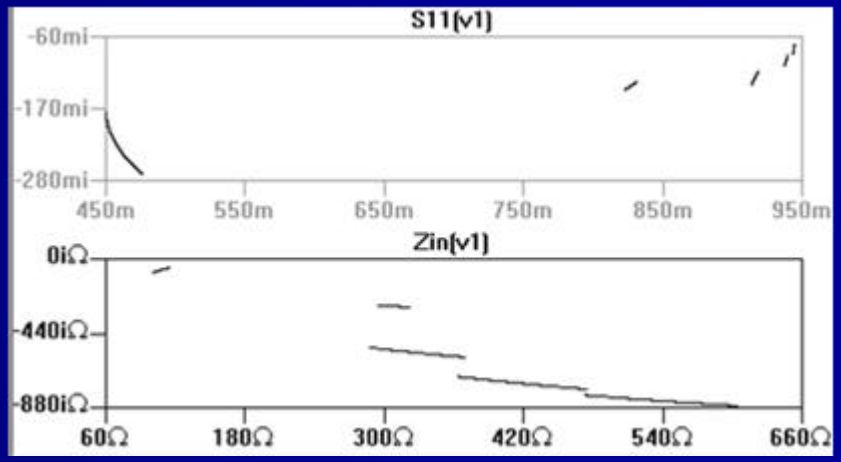
- CC s-parameters
- CE Stability
- F/T domain response



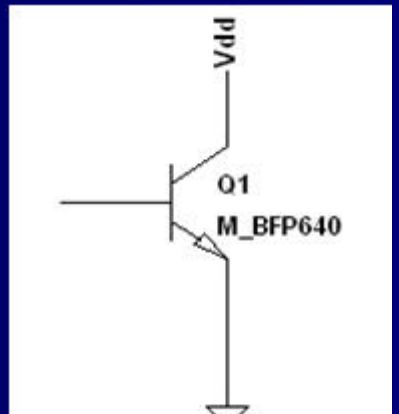

CC s-parameters

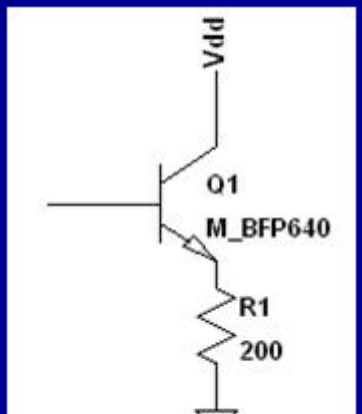


Common emitter



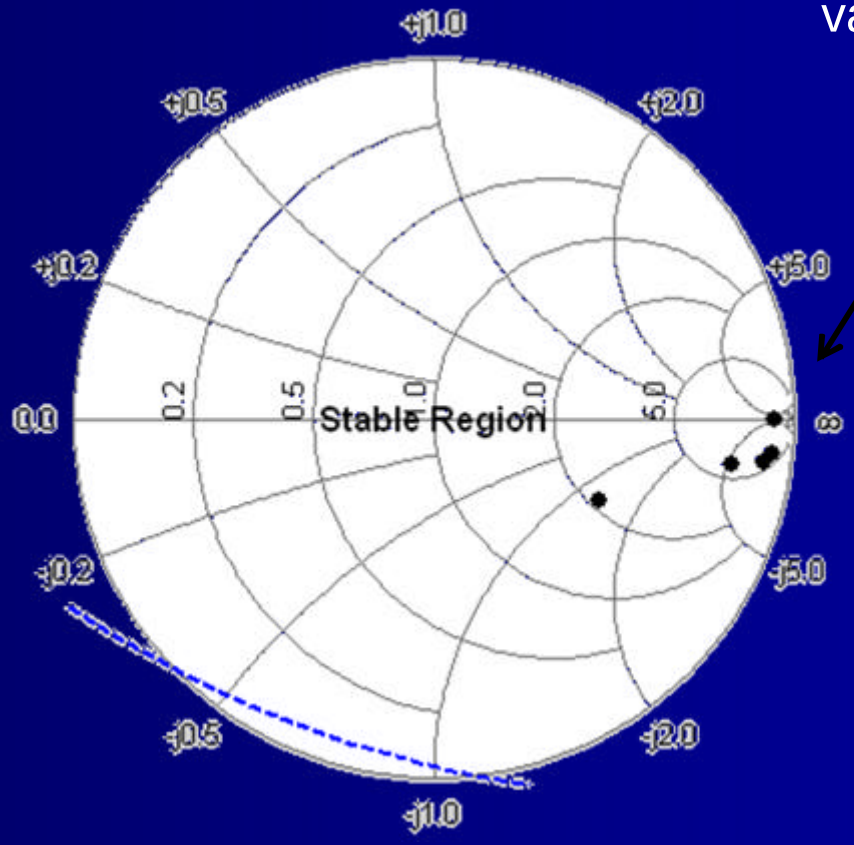
Common collector





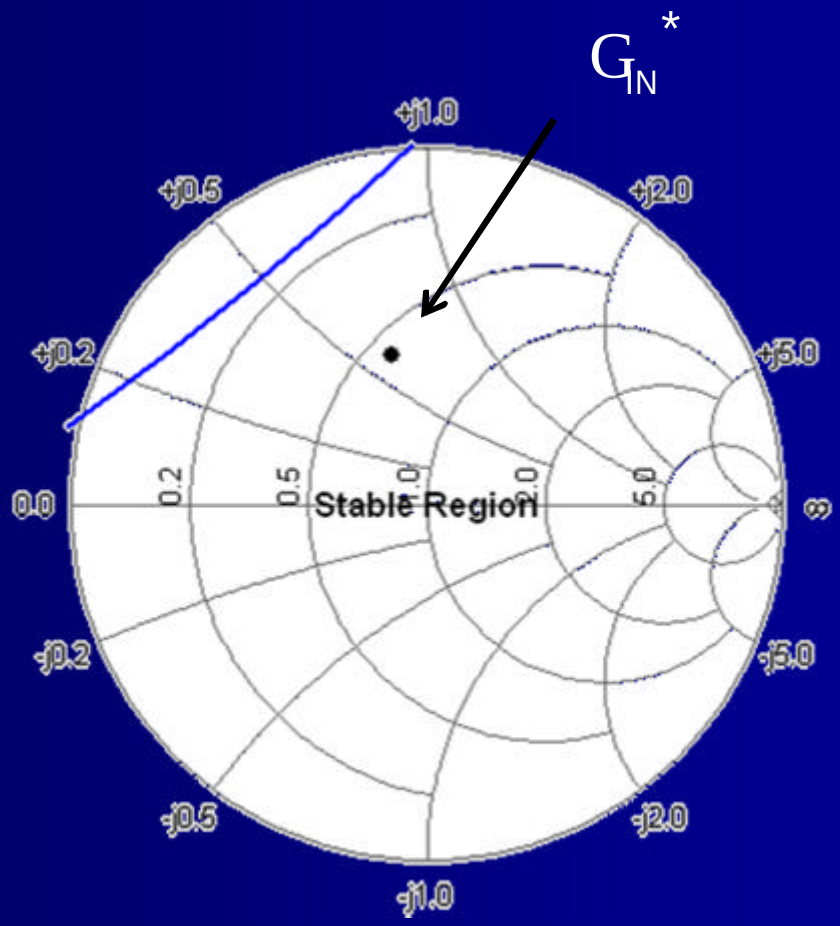
CE Stability

CE load with variable current



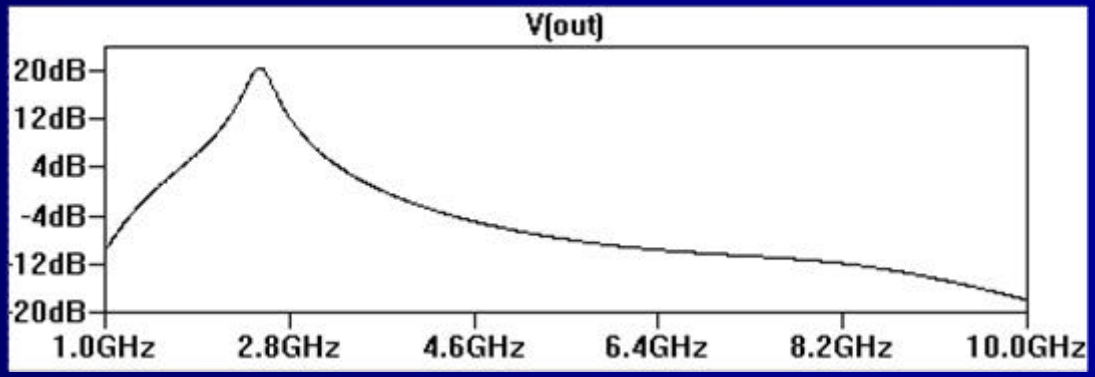
CE Output stability circle

CE Stability

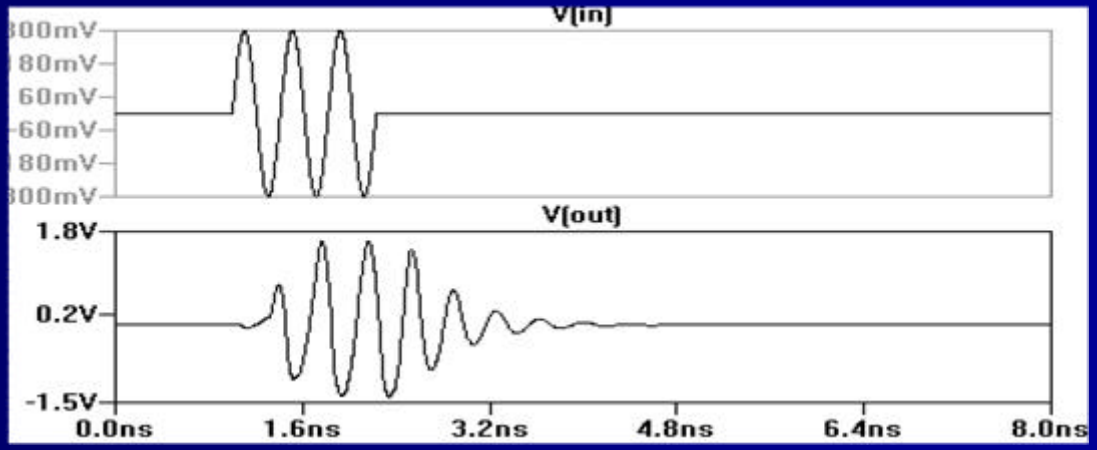


CE Intput stability circle

F/T-domain response



F-domain



T-domain

Introduction / objectives

Design

Simulations

Conclusions / future work and questions

Conclusions

- Of shelf RF PA IC has been fully implemented and manufactured
- Transistor level design RF PA has been designed with Spice and Matlab RF toolbox
- Spice simulations showed an efficiency of 55% @ 20mW

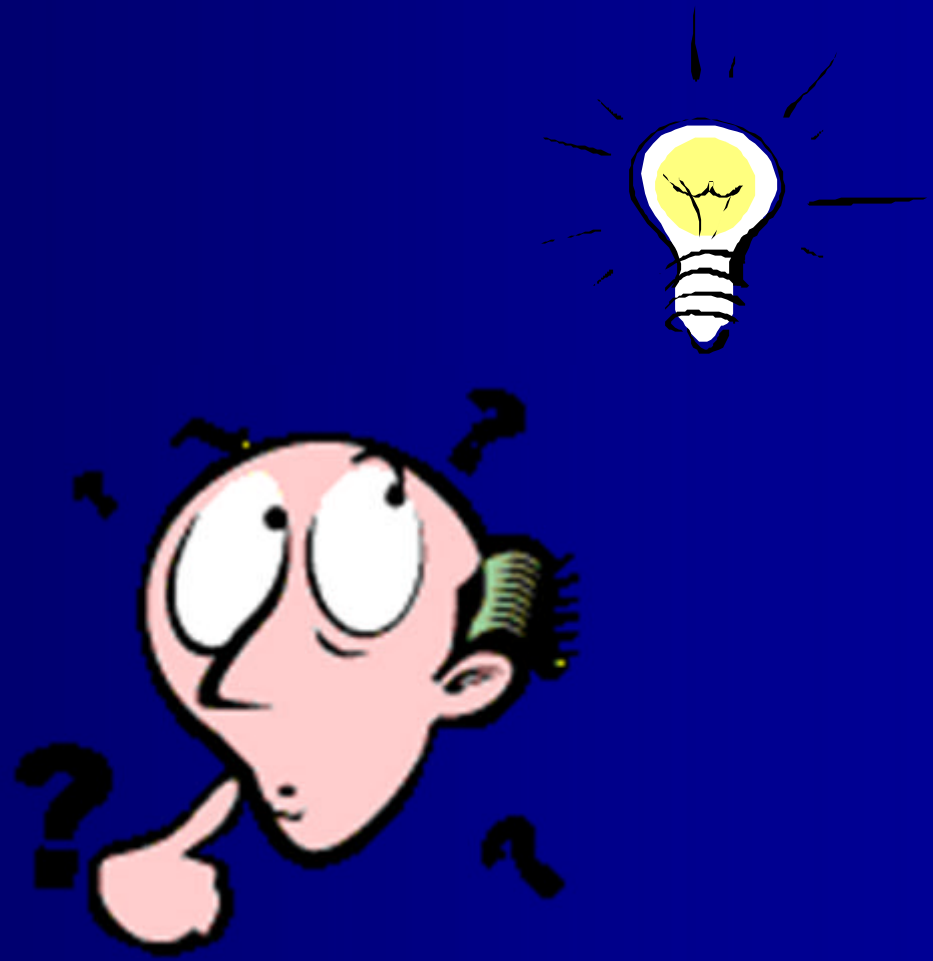


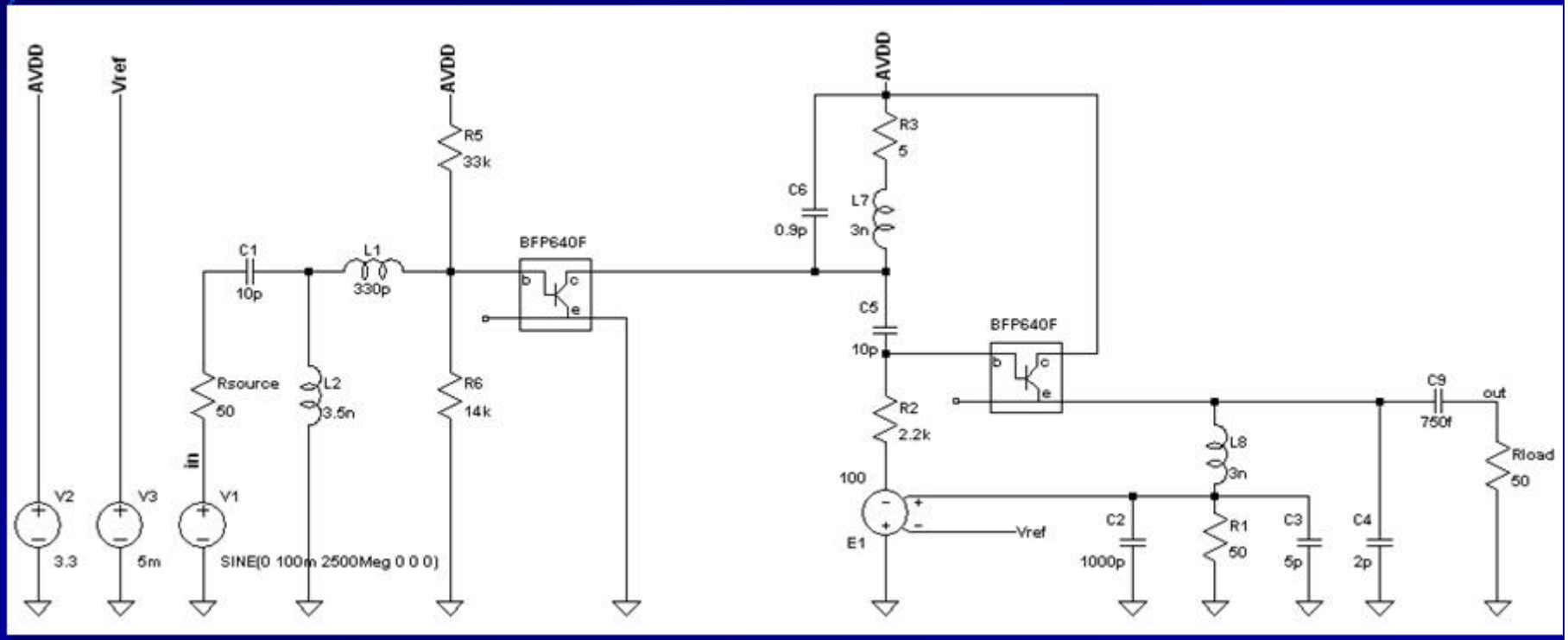

Future work

- RF switches have to be selected
- Spice simulation have to be checked once more including non ideal linear components
- A layout of the transistor level design has to be made
- The two designed PA's will be measured, compared and checked if they are on spec.
- After the measurements it might be necessary to reiterate the design




Questions





$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots$$